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Docket No.: GR 97 P 1903

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MAIL STOP: APPEAL BRIEF-PATENTS

By: Hongbing Chen Date: December 9, 2005

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
Before the Board of Patent Appeals and Interferences

Applic. No.	:	09/483,737 Confirmation No.: 8769
Inventor	:	Hansjörg Reichert
Filed	:	January 14, 2000
Title	:	Method and Apparatus for Producing a Chip-Substrate Connection
TC/A.U.	:	2826
Examiner	:	Ahmed N Sefer
Customer No.	:	**24131**

Hon. Commissioner for Patents
Alexandria, VA 22313-1450

Supplemental Appeal Brief

S i r :

In response to the final Office action dated September 9, 2005, in which the Examiner reopened the prosecution, Appellants request reinstatement of the appeal and submit this Supplemental Appeal Brief.

Real Party in Interest:

This application is assigned to Infineon Technologies AG of München, Germany. The assignment will be submitted for recordation upon the termination of this appeal.

Related Appeals and Interferences:

There are no prior or pending appeals, interferences or judicial proceedings which may be related to, directly affect or be directly affected by or have a bearing on the Board's decision in this appeal.

Status of Claims:

Claim 15 is rejected and is under appeal. Claims 2-8 were cancelled in an amendment dated October 25, 2004. Claims 11-14 and 16 were cancelled in an amendment dated January 24, 2002. Claim 17 was cancelled in an amendment dated April 11, 2003. Claims 1 and 9-10 were withdrawn from consideration.

Status of Amendments:

No claims were amended after the final Office action. A *Notice of Appeal* was submitted on April 7, 2005. A *Brief on Appeal* was submitted on June 3, 2005.

Summary of the Claimed Subject Matter:

The invention of the instant application relates to a semiconductor component. The semiconductor component includes a solder containing at least two components with at least two metal-containing constituents including a first constituent X being formed of a precious metal and a second constituent Y being consumed during a soldering operation by one of reacting and being dissolved in materials which are to be joined. See page 1, lines 12-16 of the specification. The solder has a hypereutectic concentration of the second constituent Y. See page 7, lines 24-26 of the specification. The semiconductor component further includes a substrate (2) and a semiconductor chip (1) having a rear side and an adhesive or diffusion barrier (4) provided on the rear side. The semiconductor chip is secured at the rear side of the semiconductor chip to the substrate by alloying or brazing using the solder to form a chip-substrate connection by the solder. See page 8, line 23 to page 9, line 5 of the specification as well as Figs. 2A and 2B. The solder contains a gold-tin compound (AuSn) having a composition by weight of Au to Sn of 70 to 30 and forming a layer having a thickness of from about 1 μm to about 2 μm. See page 6, lines 5-10 and page 9, line 7 of the specification.

References Cited:

JP 6-326210	Ishii	November 25, 1994
5,234,153	Bacon et al.	August 10, 1993
WO 88/03705	Fister et al.	May 19, 1988

Grounds of Rejection to be Reviewed on Appeal

1. Whether or not claim 15 is obvious over Ishii in view of Fister et al. and Bacon et al. under 35 U.S.C. §103(a).

Argument:

Claim 15 is not obvious over Ishii in view of Fister et al. and Bacon et al. under 35 U.S.C. §103(a).

In item 3 on pages 2-4 of the above-mentioned Office action, claim 15 has been rejected as being unpatentable over Ishii in view of Fister et al. and Bacon et al. under 35 U.S.C. § 103(a).

Before discussing the prior art in detail, it is believed that a brief review of the invention as claimed, would be helpful.

Claim 15 calls for, inter alia:

> a semiconductor chip having a rear side and an adhesive or diffusion barrier provided on said rear side;

said semiconductor chip being secured at said rear side to said substrate by one of alloying and brazing using said solder to form a chip-substrate connection by said solder.

According to the invention of the instant application, an adhesive or diffusion barrier (4) is provided on the rear side of the semiconductor chip (1), which is then secured to the substrate (2) by a solder (5) (see Fig. 2B).

Ishii discloses a sub-mount interposed between a laser chip 1 and a metal block 5. As can be seen from Fig. 2 of Ishii, there is a barrier layer 7a between the chip 1 and the substrate 40. However, the solder 8 is provided between the chip 1 and the barrier layer 7a, not between the barrier layer 7a and the substrate 40. Therefore, Ishii does not disclose "an adhesive or diffusion barrier provided on said rear side" and "said semiconductor chip being secured at said rear side to said substrate by one of alloying and brazing using said solder to form a chip-substrate connection by said solder," as recited in claim 15 of the instant application.

Fister et al. disclose in Fig. 1 a semiconductor die 12, an adhesive 19 on the rear side of the die 12, a substrate 14, and a solder 18. However, the solder 18 does not form a chip-substrate connection. Rather, the solder 18 is provided between the buffer component 16 and the substrate 14.

Although Fig. 5 of Fister et al. shows a chip 12'''-substrate 14''' connection by the solder 18''', it does not show an adhesive or diffusion barrier provided on the rear side of the chip.

The reference Bacon et al. was cited by the Examiner as teaching the advantages of using a thin gold-tin compound solder. In fact, Bacon et al. also do not disclose "an adhesive or diffusion barrier provided on said rear side" and "said semiconductor chip being secured at said rear side to said substrate by one of alloying and brazing using said solder to form a chip-substrate connection by said solder," as recited in claim 15 of the instant application.

Clearly, none of the cited references shows "an adhesive or diffusion barrier provided on said rear side" and "said semiconductor chip being secured at said rear side to said substrate by one of alloying and brazing using said solder to form a chip-substrate connection by said solder," as recited in claim 15 of the instant application.

It is accordingly believed to be clear that none of the references, whether taken alone or in any combination, either

show or suggest the features of claim 15. Claim 15 is, therefore, believed to be patentable over the art.

In view of the foregoing, the honorable Board is therefore respectfully urged to reverse the final rejection of the Primary Examiner.

Respectfully submitted,

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Claims Appendix:

15. A semiconductor component, comprising:

a solder containing at least two components with at least two metal-containing constituents including a first constituent X being formed of a precious metal and a second constituent Y being consumed during a soldering operation by one of reacting and being dissolved in materials which are to be joined, and said solder having a hypereutectic concentration of said second constituent Y;

a substrate; and

a semiconductor chip having a rear side and an adhesive or diffusion barrier provided on said rear side;

said semiconductor chip being secured at said rear side to said substrate by one of alloying and brazing using said solder to form a chip-substrate connection by said solder;

said solder containing a gold-tin compound (AuSn) having a composition by weight of Au to Sn of 70 to 30 and forming a layer having a thickness of from about 1 μm to about 2 μm.

Evidence Appendix:

No evidence pursuant to §§ 1.130, 1.131, or 1.132 or any other evidence has been entered by the Examiner and relied upon by appellant in the appeal.

Related Proceedings Appendix:

Since there are no prior or pending appeals, interferences or judicial proceedings which may be related to, directly affect or be directly affected by or have a bearing on the Board's decision in this appeal, no copies of decisions rendered by a court or the Board are available.